

REMARKS

Claims 1, 3-5, 7-9, 11-13, 15-18 are pending. Claims 6 and 10 have been canceled. Claims 3 and 15 have been amended for clarity only. Reconsideration and allowance of the present application based on the following remarks are respectfully requested.

In accordance with the telephone conference with Examiner Mondt on May 13, 2002, a personal interview has been scheduled on May 20, 2002 to discuss the Amendment provided herein.

In the Drawings

The drawings are objected to because of a typographical error in Figures 3 and 4B. Applicant has submitted a Request for Approval of Drawing Corrections to correct the drawings in accordance with the suggestions in the Office Action. Accordingly, Applicant respectfully requests withdrawal of the objection.

Claim Objections

Claims 6 and 10 are objected to for being identical to claims 5 and 9 respectively. Accordingly, claims 6 and 10 have been canceled without prejudice or disclaimer and therefore, Applicant respectfully requests withdrawal of the objection.

Additionally, claims 3 and 15 have been amended to replace the term "ladder-like" with --ladder-shaped--.

Claim Rejections Under 35 U.S.C. § 103

Claims 1, 3-13, 15 and 16 were rejected under 35 U.S.C. § 103(a) over Yamada (U.S. Patent No. 5,502,320) in view of Hshieh et al (U.S. Patent No. 5,986,304). This rejection is moot with respect to claims 6 and 10 because of the cancellation of those claims and Applicant respectfully traverses this rejection with respect to claims 1, 3-5, 7-9, 11-13, 15 and 16.

Independent claim 1 recites, in part, that the semiconductor device comprises a plurality of trench gates extending through the body region. The Examiner admits that this feature is not taught by Yamada, however the Examiner alleges that Hshieh teaches this feature and that it would have been obvious to combine the two references. Further the Examiner correctly indicates that the device of Yamada is not necessarily designed to

withstand a high voltage. Applicant notes that the device of Yamada is a DRAM memory device and therefore would not be concerned with being able to withstand a high voltage. Therefore, there would be no motivation to combine the teachings of Yamada with those of Hshieh since Yamada is not concerned with high voltages or punch through.

Additionally, even if there was a motivation to combine Yamada with Hshieh, Yamada teaches away from the trench gate extending through the body region. For example, Yamada shows a linear element isolation trench 3 which is formed in the substrate 1. Additionally, the linear gate trench 5 is formed in the substrate 1. Yamada further teaches that "it is preferable to form the gate trench 5, with a smaller depth than the element isolation trench 3 so as to maintain the element isolation ability of the isolation trench 3 high" (Figure 6B, column 7, lines 20-23). Therefore, Yamada teaches away from extending the gate trench past the isolation trench and accordingly through the body region.

Independent claim 13 recites, in part, a process for producing a semiconductor device comprising forming a plurality of trench gates extending through the body region. Applicant submits that claim 13 is allowable for the same reasons presented above with regard to claim 1.

Claims 3-5, 7-9, 11,12, 15 and 16 are believed allowable by virtue of their dependence from claims 1 and 13 for at least the reasons presented above with regard to claims 1 and 13. Accordingly, Applicant respectfully requests that the rejection be withdrawn.

Conclusion

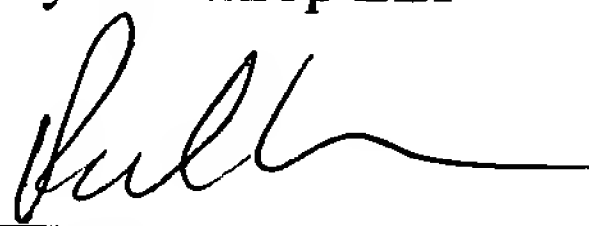
Applicant appreciates that claims 17 and 18 have not been rejected under prior art. However, in view of the foregoing, all the claims are now believed to be in form for allowance, and such action is hereby solicited. If any point remains in issue which the Examiner feels may be best resolved through a personal or telephone interview, please contact the undersigned at the telephone number listed below.

Attached is a marked-up version of the changes made to the claims by the current amendment. The attached Appendix is captioned **"Version with markings to show changes made"**.

All objections and rejections having been addressed, it is respectfully submitted that the present application is in a condition for allowance and a Notice to that effect is earnestly solicited.

Respectfully submitted,

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Enclosures: Appendix

Request for Approval of Drawing Corrections with Figures 3 and 4B

APPENDIX

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Claims 3 and 15 have been amended as follows:

3. (Twice Amended) A semiconductor device according to claim 1, wherein the first semiconductor regions are formed along the trench gates, and the second semiconductor regions connect the first semiconductor regions formed between the trench gates so as to form a [ladder-like] ladder-shaped configuration.

15. (Twice Amended) A process according to claim 13, wherein the first semiconductor regions are formed along the trench gates, and the second semiconductor regions connect the first semiconductor regions formed between the trench gates so as to form a [ladder-like] ladder-shaped configuration.

End of Appendix